We claim:

1. An interconnect structure formed on a substrate, the structure comprising:

a dielectric layer overlying the substrate, said dielectric layer being formed of a carbon-containing dielectric material having a dielectric constant of less than about 4;

a continuous hardmask layer on said dielectric layer, said hardmask layer having a top surface;

at least one conductor embedded in said dielectric layer and having a surface coplanar with the top surface of said hardmask layer; and

a cap layer on said at least one conductor and on said hardmask layer, said cap layer having a bottom surface in strong adhesive contact with said conductor, wherein said cap layer is formed of silicon nitride by a plasma-enhanced chemical vapor deposition (PE CVD) process.

2. The interconnect structure according to Claim 1, further comprising a pre-clean layer disposed beneath said cap layer and on said at least one conductor and said hardmask layer, said pre-clean layer being formed of a material comprising copper, silicon and oxygen.

3. The interconnect structure according to Claim 1, further comprising a conductive liner disposed between said conductor and said dielectric layer.

4. The interconnect structure according to Claim 1, further comprising an adhesion promoter layer disposed between said dielectric layer and the substrate.

5. The interconnect structure according to Claim 1, wherein said dielectric layer is formed of an organic thermoset polymer having a dielectric constant of about 1.8 to about 3.5.

6. The interconnect structure according to Claim 5, wherein said dielectric layer is formed of a polyarylene ether polymer.

7. The interconnect structure according to Claim 1, wherein said hardmask layer is formed of silicon nitride.

8. The interconnect structure according to Claim1, wherein said hardmask layer is formed of silicon carbide.

9. The interconnect structure according to Claim 1, wherein said conductor is formed of copper.

10. The interconnect structure according to Claim 1, wherein said hardmask layer has a thickness of at least about 500 angstroms.

11. The interconnect structure according to Claim 7, wherein said hardmask layer has a thickness of at least about 25 angstroms.

12. The interconnect structure according to Claim 8, wherein said hardmask layer has a thickness of at least about 100 angstroms.

13. The interconnect structure according to Claim 1, wherein said cap layer has a thickness of about 5 to about 120 nm.

14. The interconnect structure according to Claim 1, wherein said cap layer has a composition of about 30 to 45 atomic % silicon, about 30 to 55 atomic % nitrogen, and about 10 to 25 atomic % hydrogen.

15. A method for forming an interconnect structure on a substrate, the method comprising the steps of:

depositing a dielectric layer, said dielectric layer being formed of a carbon-containing dielectric material having a dielectric constant of less than about 4;

depositing a hardmask layer on said dielectric layer, said hardmask layer having a top surface;

forming an opening in said dielectric layer and said hardmask layer;

filling said opening with a conductive material, thereby forming a conductor, said conductor having a surface coplanar with the top surface of said hardmask layer;

exposing said conductor to a reducing plasma comprising at least one gas selected from the group consisting of H_2, N_2, NH_3 and noble gases; and

depositing silicon nitride on said conductor by a plasma-enhanced chemical vapor deposition (PE CVD) process, thereby forming a silicon nitride cap layer.

16. The method according to Claim 15, wherein said hardmask layer is formed of silicon nitride, and is deposited by a chemical vapor deposition (CVD) process.

17. The method according to Claim 15, wherein said hardmask layer is formed of silicon carbide, and is deposited by a chemical vapor deposition (CVD) process.

18. The method according to Claim 15, wherein said conductor is exposed to a reducing plasma comprising NH_3 at a flow rate of at least about 4000 sccm.

19. The method according to Claim 15, wherein said conductor is exposed to a reducing plasma with a high frequency RF power of about 150 watts to about 450 watts and a low frequency RF power of about 100 watts to about 300 watts.

20. The method according to Claim 15, wherein said conductor is exposed to a reducing plasma in a chemical vapor deposition (CVD) reactor at a pressure of less than about 20 torr, and said silicon nitride cap layer is deposited in the same CVD reactor at a pressure of less than about 10 torr.